This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Original) A system for aligning data transferred across circuit boundaries having different clock domains, wherein a first clock signal operates in a first clock domain and a second clock signal operates in a second clock domain, said first and second clock signals of the same frequency but operating out of phase, said system comprising:

a buffer circuit comprising latch means receiving data clocked in said first clock domain and latching said received data in said second clock domain by one of a first edge of said second clock signal, or a second opposite edge of said second clock signal; and,

a control circuit means for receiving said first and second clock signals and determining a phase relationship therebetween, said control circuit generating a control signal based on said determined phase relationship, said control signal implemented for selecting one of said first edge of said second clock signal, or said second opposite edge of said second clock signal, for said latch means latching action in said second clock domain,

wherein reliable data transfer operation is provided for all possible phase relationships of said first and second clock signals.

2. (Original) The system as claimed in Claim 1, wherein said latch means comprises:

a first latch device for receiving said data clocked in said first clock domain and clocked in said second clock domain, said first latch device generating a latched data output; and,

a second latch device for receiving one of said received data clocked in said first clock domain or said latched data output from said first latch device in accordance with said control signal.

3. (Original) The system as claimed in Claim 2, further comprising:

a multiplexor device receiving both said received data clocked in said first clock domain or said latched data output from said first latch device and selecting either of said received data clocked in said first clock domain or said latched data output from said first latch device in accordance with said control signal.

4. (Original) The system as claimed in Claim 3, wherein each said first and second latch devices comprise an edge- triggered flip-flop device, a first edge of said second clock signal comprising one of a rising edge or falling edge, and said second clock edge comprising an opposite edge.

5. (Original) The system as claimed in Claim 3, wherein a phase of said second clock signal is similar in phase to said first clock signal, said control signal enabling said second latch device to receive said latched data output from said first latch device.

6. (Original) The system as claimed in Claim 3, wherein a phase of said second clock signal is opposite in phase to said first clock signal, said control signal enabling said second latch device to receive said received data clocked in said first clock domain.

7. (Original) The system as claimed in Claim 3, wherein said control circuit comprises:

means for receiving said first clock signal and generating a delayed first clock signal;

a first data synchronization path comprising two or more serially connected latch devices, a first latch device thereof receiving said delayed first clock signal, each of said serially connected latch devices latched in by an edge of said second clock signal and generating first set of output signals thereof;

a second data synchronization path comprising two or more serially connected latch devices, a first latch device thereof receiving said delayed first clock signal, each of said serially connected latch devices latched in by an opposite edge of said second clock signal and generating a second set of output signals thereof; and,

a logic means receiving said first and second output signal sets and generating said control signal.

8. (Original) The system as claimed in Claim 7, wherein said logic means comprises a finite state machine implementing logic for generating said control signal.

9. (Original) The system as claimed in Claim 7, wherein said delayed first clock signal is delayed about ¾ of a clock cycle with respect to said first clock signal.

10. (Original) The system as claimed in Claim 7, wherein said first synchronization path further comprises logic devices for receiving a latched output from each said two or more serially connected latch devices in said first path and generating first and second logic output signals therefrom, and said second synchronization path further comprises logic devices for receiving a latched output from each said two or more serially connected latch devices in said second path and generating third and fourth logic output signals therefrom, said finite state machine receiving each said first, second third and fourth logic output signals and applying a Boolean equation to generate said control signal.

11. (Original) The system as claimed in Claim 1, wherein data is transferred across said circuit boundaries over an n-bit data path, said system comprising n buffer circuits, one buffer circuit for each data bit.

12. (Original) A system for aligning data transferred over an n-bit wide data path across circuit boundaries having different clock domains, wherein a first clock signal operates in a first clock domain and a second clock signal operates in a second clock domain, said first and second clock signals of the same frequency but operating out of phase, said system comprising:

n buffer circuits each for receiving a single data bit of said n-bit wide path, each buffer circuit comprising a latch means for receiving data clocked in said first clock domain and latching said received data in said second clock domain by one of a first edge of said second clock signal, or a second opposite edge of said second clock signal; and,

a control circuit means for receiving said first and second clock signals and determining a phase relationship therebetween, said control circuit generating a control signal based on said determined phase relationship, said control signal implemented in each of said n buffer circuits for selecting one of said first edge of said second clock signal, or said second opposite edge of said second clock signal, for said latch means latching action in said second clock domain,

wherein reliable data transfer operation is provided for all possible phase relationships of said first and second clock signals.

13. (Original) The system as claimed in Claim 12, wherein said latch means of each buffer circuit comprises:

a first latch device for receiving said data clocked in said first clock domain and clocked in said second clock domain, said first latch device generating a latched data output; and,

a second latch device for receiving one of said received data clocked in said first clock domain or said latched data output from said first latch device in accordance with said control signal.

14. (Original) The system as claimed in Claim 13, wherein each buffer circuit further comprises:

a multiplexor device for receiving both said received data clocked in said first clock domain or said latched data output from said first latch device and selecting either of said received data clocked in said first clock domain or said latched data output from said first latch device in accordance with said control signal.

15. (Original) The system as claimed in Claim 14, wherein said control circuit comprises:

means for receiving said first clock signal and generating a delayed first clock signal;

a first data synchronization path comprising two or more serially connected latch devices, a first latch device thereof receiving said delayed first clock signal, each of said serially connected latch devices latched in by an edge of said second clock signal and generating first set of output signals thereof;

a second data synchronization path comprising two or more serially connected latch devices, a first latch device thereof receiving said delayed first clock signal, each of said serially connected latch devices latched in by an opposite edge of said second clock signal and generating a second set of output signals thereof; and,

a logic means receiving said first and second output signal sets and generating said control signal.

16. (Original) A method for aligning data transferred across circuit boundaries having different clock domains, wherein a first clock signal operates in a first clock domain and a

second clock signal operates in a second clock domain, said first and second clock signals of the same frequency but operating out of phase, said method comprising the steps of:

a) receiving data supplied from a from a first clock domain circuit clocked by said first clock signal;

b) determining a phase relationship between said first and second clock signals; and,

c) latching said received data in said second clock domain by one of a first edge of said second clock signal, or a second opposite edge of said second clock signal based on said determined phase relationship,

wherein reliable data transfer operation is provided for all possible phase relationships of said first and second clock signals.

17. (Original) The method as claimed in Claim 16, wherein said determining step b) comprises the steps of:

receiving said first clock signal and generating a delayed first clock signal;

inputting said delayed first clock signal to a first latch device of a first data synchronization path comprising two or more serially connected latch devices clocked by an edge of said second clock signal in said second clock domain and generating a first set of output signals thereof;

simultaneously inputting said delayed first clock signal to a first latch device of a second data synchronization path comprising two or more serially connected latch devices clocked by an opposite edge of said second clock signal in said second clock domain and generating a second set of output signals thereof; and,

applying logic to said first and second set of output signals for determining said phase relationship.

18. (Original) The method as claimed in Claim 17, wherein said latching step c) comprises the steps of:

latching data in said first clock domain by a first latch device clocked by said first clock signal and providing first latched data output;

inputting said first latched data output to a second latch device clocked by a second clock signal and providing second latched data output;

selecting said first latched data output and second latched data output based on said phase relationship; and,

inputting said selected first latched data output or second latched data output to a third latch device clocked by an opposite edge of said second clock signal.

19. (Original) The method as claimed in Claim 18, wherein said first latched data output is selected for input to said third latch device when a phase of said second clock signal is similar in phase to said first clock signal, and said second latched data output is selected for input to said third latch device when a phase of said second clock signal is opposite in phase to said first clock signal.

20. (Currently Amended) A single stage clock crossing buffer for aligning data transferred across circuit boundaries having different clock domains, wherein a first clock signal operates in a first clock domain and a second clock signal operates in a second clock domain, said first and second clock signals of the same frequency but operating out of phase, the buffer comprising:

first latch means for receiving data supplied from a from a first clock domain circuit and clocked by said first clock signal to generate a latched output thereof;

means for determining a phase relationship between said first and second clock signals; and,

second latch means for latching said latched output in said second clock domain by one of a first edge of said second clock signal, or a second opposite edge of said second clock signal based on said determined phase relationship, wherein reliable data transfer operation is provided for all possible phase relationships of said first and second clock signals.